REMARKS

Claims 1-37 are pending in this application, of which claims 1, 11, 21, 24, 27, and 30 are independent. Applicant has amended the independent claims merely to clarify claim terms and not to add limitations, and therefore submits that a new search is not necessary. For instance, claim 1 now recites "...executable instructions to be executed on a multithreaded engine included in a packet processor ..." However, the addition of the word "executable" has already been considered by the examiner since the claim previously recited "instructions executed on a multithreaded engine included in a packet processor. Thus, this is a mere clarification and no further search or consideration is required.

The examiner rejected claims 1-2, 4-5, 11-12, 14-15, 21-22, 24-25, 27-28, 30-31, and 33-37 under 35 USC 103 for obviousness over Pereira in view of Wolrich.

In rejecting claims 1 and 11, the examiner stated:

> **As per claims 1 and 11, Pereira discloses allocating a memory entry in a memory device to instructions, with a portion of the memory entry including a unique identifier assigned to the instructions (col. 7, lines 7-21; col. 18, lines 36-39; Fig. 6, element 190).** ***It should be noted that computer program product in claims 11-20 executes the exact same functions as the methods in claims 1-10. Therefore, any references that teach claims 1-10 also teach the corresponding claims 11-20. It should be noted that the instructions within the packets of the "IPv4 pools, IPv6 pools, and MPLS pools" are analogous to the "instructions." It should also be noted that the "hash CAM blocks" are analogous to "memory entries allocated to instructions." Lastly, it should be noted that the "entry type value is analogous to the "unique identifier."***
>
> **Pereira does not expressly disclose a multithreaded engine included in a packet processor.**
>
> **Wolrich discloses a multithreaded engine included in a packet processor (paragraph 0014, lines 2-7; paragraph 012, lines 1-4; Fig. 2, elements 18 and 21).** ***It should be noted that the "network processor" is analogous to the "packet processor."***

Further, the examiner stated:

> **An IPv4 pool consists of IPv4 packets, an IPv6 pool consists of IPv6 packets, and an MPLS pool consists of MPLS packets. The "protocol" field of an IPv4 packet header contains instructions, the "next header" field of an IPv6 packet header contains instructions, and the "label" field of an MPLS packet header contains instructions. Accordingly, Pereira sufficiently discloses allocating a memory entry in a memory device to instructions.**

Applicant disagrees that Pereira discloses allocating memory to "instructions" as used in the specification. For example, Applicant points out that "[i]nstructions executed on the packet engine 46 are typically written in code designed for the network processor 22 and the code is typically referred to as microcode. However, in some arrangements, high-level languages such as "C", "C++" or other similar computer languages are used to program instructions for execution on the packet engine 46" (Applicant's Specification, page 7, lines 14-19).

To the contrary, the IPv4 packets, IPv6 packets, and MPLS packets disclosed in Pereira do not contain "executable instructions" (or the previously recited "instructions executed on a multithreaded engine") to which a memory entry is allocated. Although not specifically disclosed in Pereira, the examiner notes that the header sections of IPv4 packets, IPv6 packets, and MPLS packets contain "protocol" fields, "next header" fields, and "label" fields, respectively. These fields, however, merely serve to indicate the protocol of the data contained in the payloads of such packets. Indeed, indication of protocol cannot, and should not, be interpreted to cover instructions or executable instructions. Applicant therefore submits that Pereira neither discloses nor suggests "executable instructions," as recited in claim 1.

The examiner cites Wolrich solely for its disclosure of "a multithreaded engine included in a packet processor." Even if Pereira and Wolrich are combined in the manner suggested by the examiner, the combination still does not disclose or suggest all of the features of claim 1. For at least these reasons, claim 1 is allowable over Pereira and Wolrich.

Claims 11, 21, 24, and 27 contain similar limitations as claim 1 and are patentable for at least the same reasons.

> **As per claim 30, Pereira discloses a method comprising:**
>
> **allocating a content-addressable-memory (CAM) entry to a microblock, with a portion of the CAM entry including a unique identifier assigned to the microblock (col. 7, lines 7-21; col. 18, lines 36-49; Fig. 6, element 190).** ***It should be noted that each "pool" is analogous to a "microblock."***
>
> **Pereira does not expressly disclose a multithreaded microengine included in a network processor.**
>
> **Wolrich discloses a multithreaded microengine included in a network processor (paragraph 0014, lines 2-7; paragraph 0012, lines 1-4; Fig. 2, elements 18 and 21).**

Applicant points out that microblocks are blocks of executable instructions, i.e., microcode (Applicant's Specification, page 7, line 22). As discussed above, Pereira neither

discloses nor suggests "executable instructions." Applicant submits, therefore, that Pereira also neither discloses nor suggests an "executable microblock," as recited in claim 30.

The examiner cites Wolrich solely for its disclosure of "a multithreaded engine included in a packet processor." Even if Pereira and Wolrich are combined in the manner suggested by the examiner, the combination still does not disclose or suggest all of the features of claim 30. For at least these reasons, claim 30 is allowable over Pereira and Wolrich.

All dependent claims are patentable for at least the same reasons as the claims on which they depend.

In view of the foregoing amendments and remarks, the entire application is believed to be in condition for allowance, and such action is respectfully requested.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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